

SIVIA SEMICONDUCTOR

Intelligent Hardware. Reliable Systems.

STARTUP PROFILE

Semiconductor IP • Hardware Reliability • Fault-Aware Computing

A deep-tech, fabless semiconductor IP startup incubated at VIT Technology Business Incubator (VIT-TBI), Vellore, India.

Company overview based on Sivia Semiconductor's autonomous-systems reliability and High Bandwidth Flash (HBF) R&D; proposals.

01 | Who We Are

Sivia Semiconductor is a deep-tech, fabless semiconductor IP startup focused on developing intelligent, lightweight, and reusable hardware IP for reliability-aware computing. Its central direction is to help semiconductor-based systems move beyond basic pass/fail fault handling toward graded health assessment, early risk detection, and coordinated responses to hardware degradation.

The proposals describe a common reliability approach applied to two important domains: autonomous aerial systems and AI memory infrastructure. Rather than positioning Sivia as a drone manufacturer or a conventional chip fabrication company, the emphasis is on reusable IP architectures that can be integrated into FPGA, SoC, processor, memory, and embedded platforms.

Focus Areas

Semiconductor IP	Hardware Reliability
RTL-based, reusable hardware blocks designed to support integration across platforms.	Health telemetry, anomaly scoring, fault classification, and system-aware responses.
Memory Reliability	Autonomous Systems
ECC telemetry, adaptive testing, and reliability strategies for memory subsystems and AI infrastructure.	Monitoring sensors, actuators, motors, and related subsystems in autonomous aerial platforms.

02 | Technology Platform

The autonomous-systems proposal outlines four connected elements:

SHAM — Sensor and Subsystem Health & Anomaly Monitor

Designed to assess telemetry from sensors, motors, actuators, and related subsystems and produce graded health or risk information rather than relying only on hard pass/fail thresholds.

AMRE — Adaptive Memory Reliability Engine

Proposed to retain and analyze ECC syndrome information, distinguish isolated upsets from recurring memory degradation, and guide targeted memory testing and repair actions.

UFML — Unified Fault-Management Layer

A common reporting and arbitration backbone intended to combine risk signals from multiple IP blocks and support transitions between full, reduced, and safe operating modes.

CMIE — Configurable Mission-Specific Intelligence Extension

A modular application extension that may be configured for use cases such as vision workload reduction, terrain/surface mapping, or communications-integrity monitoring.

03 | Reliability for AI Memory Infrastructure

Sivia’s second proposal explores an inference-aware health telemetry and reliability IP subsystem for High Bandwidth Flash (HBF) and 3D NAND memory stacks used near AI accelerators. The proposal identifies a challenge in read-heavy AI inference: memory regions may experience different levels of read exposure and data sensitivity, while generic maintenance policies can introduce unnecessary traffic, latency variation, and memory wear.

The proposed architecture observes error-correction decoder outcomes and converts them into graded, decaying health or risk scores. Host-side workload hints—such as expected read exposure and model-weight sensitivity—can inform targeted maintenance and recovery. The goal is to coordinate memory reliability actions with AI serving requirements instead of treating every memory region identically.

04 | How the Approach Is Intended to Work

1. Observe	2. Assess	3. Coordinate	4. Respond
Collect subsystem telemetry or ECC/error-correction events.	Classify anomalies and calculate a graded risk/health state.	Combine reports using a shared reliability interface.	Guide targeted testing, maintenance, recovery, or safe-mode actions.

05 | Engineering and Development Approach

- **RTL design:** Develop hardware IP using Verilog/SystemVerilog and modular microarchitectures.
- **Verification:** Use simulation, directed and randomized fault injection, and coverage-driven checks.
- **FPGA prototyping:** Evaluate functional behavior, timing, resource use, and telemetry interfaces on programmable hardware.
- **Hardware-software co-design:** Connect hardware status and risk outputs with host-side monitoring, workload information, and system control.
- **System validation:** Progress toward hardware-in-the-loop testing and platform-level evaluation with relevant partners, subject to implementation and approvals.

06 | Potential Application Areas

The proposals identify autonomous aerial systems and UAV avionics, embedded and edge systems, processor/SoC platforms, memory subsystems, High Bandwidth Flash, and AI inference infrastructure as target application areas. Actual integration and suitability depend on implementation, verification, and partner-platform requirements.

07 | Collaboration and Ecosystem

The autonomous-systems proposal describes a planned R&D; collaboration framework with TEAM ARDRA at VIT Vellore, with VIT-TBI incubation support. In that framework, Sivia's proposed contribution includes RTL IP, FPGA prototypes, reliability analytics, and verification; the partner contribution is described as UAV platforms, telemetry, and hardware-in-the-loop evaluation. Any public description of collaboration status should reflect the current approved status.

The HBF proposal describes an intended technical engagement around memory-reliability IP for advanced AI infrastructure. It should be presented publicly as a proposal or R&D; direction unless a formal partnership or product integration has been confirmed.

08 | What Differentiates Sivia

Reliability as a reusable layer

Focuses on a common architecture that can accept health and fault information from different subsystem blocks.

Graded health awareness

Aims to detect and score degradation before it becomes a binary failure condition.

Cross-domain application

Applies related reliability principles to autonomous systems and AI memory infrastructure.

Hardware-oriented implementation

Emphasizes synthesizable RTL, FPGA prototyping, verification, and integration rather than software-only monitoring.

Vendor-agnostic intent

The proposals aim for reusable interfaces that can be adapted to different processor, FPGA, SoC, and system platforms.

09 | Vision

Sivia Semiconductor aims to turn research-led reliability architectures into reusable semiconductor IP that helps computing and autonomous systems become more fault-aware, resilient, and dependable. The longer-term direction is to validate these architectures on hardware, establish practical integration interfaces, and pursue collaboration and commercialization opportunities as the technology matures.

10 | Company Snapshot

Organization	Sivia Semiconductor
Type	Deep-tech, fabless semiconductor IP startup
Incubation	VIT Technology Business Incubator (VIT-TBI), Vellore, India
Core focus	Hardware reliability IP, fault-aware computing, memory reliability
R&D; directions	Autonomous-system reliability and inference-aware HBF reliability
Website	sivia-semiconductor.in (domain owned; add a live link when website is operational)

Note: This profile summarizes the two supplied R&D; proposals. Technology descriptions refer to proposed or developing architectures and are not a claim that every module is complete, silicon-proven, flight-certified, commercially deployed, or supported by independently verified performance results.